In the Claims:

Claim 1 (currently amended): A method for decoding a first composite packet in a processor, said method comprising the steps of:

providing assembly code for each one of a plurality of instructions in a first combination of instructions in said first composite packet;

matching a template in said first composite packet to a known template corresponding to one of a plurality of known syntaxes that includes information indicating multiple stop bits that correspond to ~~an end of an issue group~~ endings of issue groups and includes information corresponding to chaining, wherein said plurality of known syntaxes are arranged as a plurality of first level nodes in a tree structure, wherein each of a plurality of second level nodes in said tree structure includes a combination of instruction types, and wherein each of a plurality of third level nodes in said tree structure includes an instruction type, wherein a plurality of paths extends between node levels and wherein each node of said plurality of first level nodes and said plurality of second level nodes has a path to a node of a different node level;

matching said one of said plurality of known syntaxes with a resolved packet syntax using said tree structure;

using said resolved packet syntax to determine assembly code associated with execution of said first combination of instructions;

providing assembly code associated with execution of said first combination of instructions.

Claim 2 (original): The method of claim 1 wherein said step of matching said one of said plurality of known syntaxes comprises the step of matching each term in said one of said plurality of known syntaxes against a respective term in said resolved packet syntax.

Claim 3 (previously presented): The method of claim 2 wherein said step of matching said one of said plurality of known syntaxes is a direct matching step.

Claim 4 (previously presented): The method of claim 1 wherein said assembly code associated with execution of said first combination of instructions specifies at least one issue group for said first combination of instructions.

Claim 5 (currently amended): The method of claim 1 wherein said assembly code associated with execution of said first combination of instructions specifies a plurality of said issue groups for said first combination of instructions.

Claim 6 (previously presented): The method of claim 1 wherein said assembly code associated with execution of said first combination of instructions identifies a

chained instruction in said first combination of instructions, wherein said chained instruction belongs to a subsequent issue group in a second composite packet.

Claim 7 (currently amended): The method of claim 1 wherein said assembly code associated with execution of said first combination of instructions identifies a plurality of chained instructions in said first combination of instructions, wherein said plurality of chained instructions belong to a respective one of said issue groups in a second composite packet.

Claim 8 (canceled).

Claim 9 (original): The method of claim 1 wherein said known template identifies at least one issue group in said first composite packet.

Claim 10 (previously presented): The method of claim 1 wherein said known template identifies a chained instruction in said first combination of instructions, wherein said chained instruction belongs to a subsequent issue group in a second composite packet.

Claim 11 (currently amended): The method of claim 1 wherein said known template identifies a plurality of chained instructions in said first combination of

instructions, wherein said plurality of chained instructions belong to a respective one of said issue groups in a second composite packet.

Claim 12 (canceled).

Claim 13 (original): The method of claim 1 wherein said composite packet in said processor consists of 128 bits.

Claim 14 (original): The method of claim 1 wherein said composite packet in said processor consists of 256 bits.

Claim 15 (original): The method of claim 1 wherein each instruction in said first combination of instructions consists of 16 bits.

Claim 16 (original): The method of claim 1 wherein each instruction in said first combination of instructions consists of 32 bits.

Claim 17 (original): The method of claim 1 wherein each instruction in said first combination of instructions consists of 41 bits.

Claim 18 (original): The method of claim 1 wherein said first combination of instructions comprises at least two instructions.

Claim 19 (original): The method of claim 1 wherein said first combination of instructions comprises at least one issue group.

Claim 20 (original): The method of claim 19 wherein said at least one issue group comprises at least one instruction.

Claim 21 (original): The method of claim 1 wherein said template comprises at least five bits.

Claims 22-31 (canceled).

Claim 32 (previously presented): The method of claim 1, wherein said instruction type is selected from a group consisting of instruction type A, instruction type I, instruction type M, instruction type F, instruction type B and instruction type LX.

Claim 33 (previously presented): The method of claim 2 wherein said step of matching said one of said plurality of known syntaxes is an indirect matching step.

Claim 34 (previously presented): The method of claim 2 wherein said step of matching said one of said plurality of known syntaxes matches each said term at one of said plurality of first level nodes in said tree structure.